Native graphene has a zero energy gap and it is therefore not suitable as a transistor channel material for digital electronics. However, recent advances based on materials engineering have demonstrated “materials on demand”, with tailored properties. Vertical heterostructures of graphene and 2D materials have been proven to be suitable for FETs and hot-electron transistors exhibiting large current modulation. Inspired by recent progress in the growth of seamless lateral 2D heterostructures, lateral heterostructure (LH)-FETs have been proposed, exhibiting extremely promising switching behavior in terms of leakage current, propagation delay, and power-delay product.

We investigate the performance and the scaling perspectives of graphene-based heterostructure FETs against the ITRS requirements for CMOS. We show that LH-FETs are very promising for high performance logic, down to the 5 nm gate length. On the other hand, vertical heterostructure FETs exhibit intrinsic delay times higher by four orders of magnitude, due to large capacitance and poor electrostatics.

We also address some fundamental aspects of off-plane transport in heterostructures of 2D materials, showing that new behaviors emerge that are not observed in the well known heterostructures based on III-V and II-VI materials systems.
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