



Invitation

to the lecture

“Vision Sensors with Pixel-Parallel Cellular Processor Arrays”

of

Dr. Piotr Dudek

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Dr. Piotr Dudek is a Reader in the School of Electrical and Electronic Engineering, The University of Manchester, leading the Microelectronics Design Lab. He received his mgr inz degree from the Technical University of Gdansk, Poland, in 1997, and the MSc and PhD degrees from the University of Manchester Institute of Science and Technology (UMIST) in 1996 and 2000 respectively. He worked as a Research Associate, and since 2002 as a Lecturer, at UMIST/The University of Manchester. During 2008/09 he was a Visiting Associate Professor in the Department of Electronic and Computer Engineering at the Hong Kong University of Science and Technology. He is the Secretary of the IEEE CAS Technical Committee on Sensory Systems, and Chair of the Neurally-Inspired Engineering Special Interest Group of the INCF UK Node. His research interests are in the area of integrated circuit design, novel computer architectures, cellular processor arrays, vision sensors and brain-inspired systems. He has published over 70 papers in these areas and received Best Paper Awards at PREP'99, IJCNN'07, CNNA'08 and CNNA'10, ISCAS'12 and Best Demo Award at ISCAS 2010.

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**Toepler-Bau, lecture room 315
Mommsenstr. 12, 01069 Dresden**

Abstract

The lecture overviews the design and implementation of vision sensors - microelectronic devices which combine image sensing and processing on single silicon die. In a way somewhat resembling the vertebrate retina these 'vision chips' perform preliminary image processing directly on the sensory plane and are capable of very high processing speed at very low power consumption. This makes them particularly suitable for embedded machine vision in applications such as autonomous robots, automated surveillance, or high-speed industrial inspection systems.

The key technologies, and concepts behind vision sensor devices will be introduced, and the lecture will be illustrated with case studies of actual CMOS vision chips implementations. The principles of using massively parallel fine-grain cellular processor arrays for low-level image processing will be presented. The analogy to topographic sensory processing networks in the mammalian brain will be elucidated. The device architectures and fundamental circuit design issues will be overviewed, and programming techniques used to map image processing algorithms onto fine grain massively parallel processor arrays will be discussed. The presented devices will include the SCAMP-5 chip, based on 256x256 array of "analogue microprocessors", and PAV-3D chip integrating sensing, analogue and digital asynchronous/synchronous processing in a separate layers of a stacked 3D CMOS technology with through-silicon vias (TSVs). The talk will include experimental results (videos) obtained with a smart-camera system based on the SCAMP vision chip in a number of vision applications including image filtering, active contour techniques, object recognition, neural networks, high-speed object tracking (image analysis at 100,000 frames per second), and ultra low-power surveillance systems.