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Microfluidic alignment and trapping of 1D nanostructures – a simple fabrication route for single-nanowire field effect transistors†

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We present a simple method to microfluidically align and trap 1D nanostructures from suspension at well-defined positions on a receiver substrate for the fabrication of single-nanowire field effect transistors (NW FETs). Our approach allows for subsequent contacting of deposited NWs *via* standard UV-lithography. We demonstrate that silicon as well as copper(II) oxide NWs can be processed, and that up to 13 out of 32 designated trapping sites are occupied with single-NW FETs.

One-dimensional (1D) nanostructures such as nanowires (NWs) can be readily synthesized in a "bottom-up" approach from metals,[1–4] organic molecules[5,6] and semiconductors.[7–28] Compared to "top-down" structures, "bottom-up" 1D nanostructures offer superior electronic properties,[7] better control in the fabrication of heterostructures with axial[1,2,8] and radial[9] variations, and smaller achievable structures down to the molecular scale.[10,11]

The great potential of "bottom-up" NWs has been demonstrated in particular in nano-electronics and -photonics, *e.g.* in field effect transistors (FETs),[7] light-emitting diodes,[8,9] microcavity lasers,[12] waveguides,[5,13] photodetectors,[6,14] and (bio-) sensors.[3,15–20] Especially for biosensing, NWs are promising building blocks, as they enable label free real-time monitoring of biologically and medically relevant data with detection limits for proteins[15–17] or DNA[18,19] down to the fM-range. The highest sensitivity is achieved employing single-NW devices,[15] which even allow for detecting single viruses,[20] and potentially single molecules.[16] To obtain multiplexed biosensors[17] that enable simultaneous monitoring of several analytes with maximized sensitivity, it is necessary to fabricate multiple single-NW devices on one chip. This, however, requires precise positioning of "bottom-up" 1D nanostructures on substrates, which is an ongoing challenge.

Several techniques – each of them with specific advantages and limitations – have been developed to arrange these nanostructures. Manipulating NWs *via* electric[4,27] or magnetic fields[1] yields single-NW devices, but is limited with regard to material choice and requires expensive equipment. Alignment approaches based on spray coating,[21] bubble-blown films,[22] Langmuir–Blodgett technique,[3,23] mechanical printing[24–26] or capillary forces[2] enable an efficient deposition of NWs over large areas, however, for reliably contacting single NWs, costly electron-beam lithography (EBL) processing is required.

When aligning 1D nanostructures *via* microfluidics, as demonstrated by Huang and co-workers, EBL is also indispensable for contacting individual NWs.[28] The deposited NWs are well oriented parallel to the liquid flow direction, yet spatial precision is limited.

The issue of full spatial control can be overcome by microfluidic trapping, as it has been demonstrated for spherically shaped, micrometer-sized particles[29] and cells.[30] In contrast, 1D nanostructures have orders of magnitude smaller diameters and significantly higher aspect ratios. Hence, the formerly presented trapping layouts are not applicable to NWs.

Here, we present a microfluidic set-up, which enables the alignment of 1D nanostructures and their trapping at designated positions. We demonstrate the deposition of single NWs

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and their subsequent contacting *via* conventional UV-lithography (UVL), making our approach simple and cost-efficient.

In our approach, we make use of the characteristic laminar flow regime of continuous-flow microfluidics and its inherent forces on rod-like structures for the alignment of NWs in flow direction.[31,32] We design a microfluidic chip that guides NWs into sufficiently narrow channels, so that an abrupt 90° change of the channel direction leads to the trapping of the 1D nano-structures. By dividing the microfluidic structure into multiple sub-channels, several NWs can be trapped in parallel. Simultaneously deposited mask alignment marks, adjacent to the trapping sites, enable a subsequent contacting of the NWs *via* UVL.

For the fabrication of our flow chambers, we use master structures fabricated in SU-8 2010 (MicroChem) and 10 μm in height, which we subsequently cast *via* soft lithography in polydimethylsiloxane (PDMS).[33] Fig. 1a depicts a schematic of the utilized master structure. The parts of the structure highlighted in dark gray form the channels for the deposition of mask alignment marks. The part of the structure highlighted in white forms the channels for aligning and trapping the NWs.

In our trapping structure the broad main channel successively branches over four stages into 32 progressively smaller sub-channels. At the trapping sites – *i.e.* the kinks in the middle of the structure – the channels are 6 μm wide. We adapt the channel widths of the intermediate branching stages according to a generalized version of "Murray's law", a biomimetic design rule based on the principle of minimum work, describing the optimum width to height ratios between parent and daughter channels in microfluidic manifolds (see also Fig. S1c†).[34,35] For drawing the NW suspension through the channels, we apply a reduced pressure of 100 mbar *via* a syringe pump at the outlet. The NWs align along the laminar flow[31,32] and are guided into the trapping sites (at t_1 in Fig. 1b). Here, the NWs cannot follow the liquid flow at the abrupt 90° change of the channel direction. Consequently, they are trapped and deposited on the receiver substrate (t_2 in Fig. 1c, see also Video in the ESI†). As a proof of concept, we trap p-doped silicon nanowires (SiNWs) of 20 μm length and 150 nm diameter (Sigma-Aldrich).

When assembling the flow set-up, it is important to prevent any distortion of the PDMS stamp and thus misalignment between trapping sites and mask alignment marks. Therefore, we place the PDMS stamp only gently on the silicon wafer receiver substrate merely utilizing the adhesion forces of the

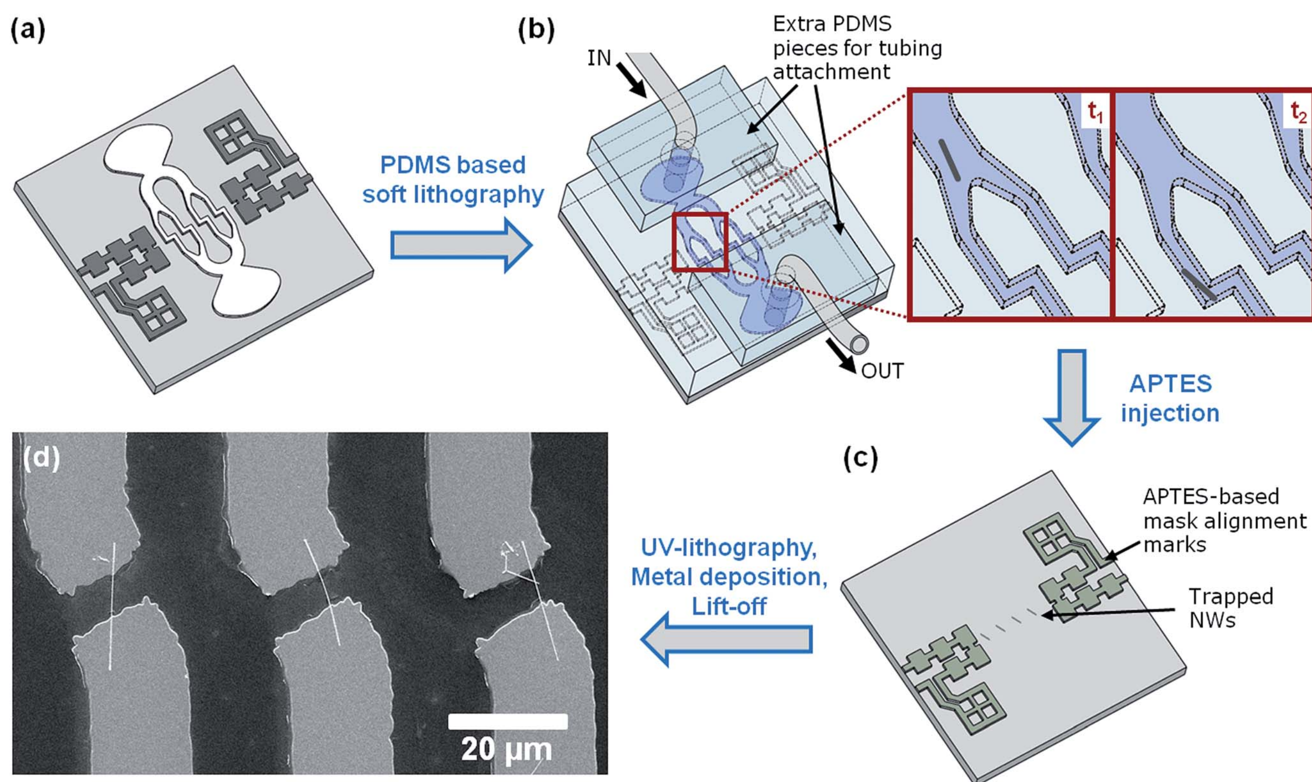

Fig. 1 Schematic of single-NW FET fabrication. (a) Fabrication of SU-8 master for soft lithographic replication with PDMS. The master contains micro-channels for NW alignment and trapping (white) and channels for depositing UVL mask alignment marks (dark grey). (b) Assembly of flow set-up for trapping NWs from suspension. Suspensions are drawn through channels under reduced pressure of 100 mbar applied *via* a syringe pump at the outlet. Tubing is first attached to extra PDMS pieces which are then bound to the PDMS stamp containing the micro-channels. In the enlarged view of the red labeled section, the process of NW trapping is shown ($t_1 < t_2$). NWs are first flow-aligned and guided into the trapping sites (t_1), then trapped and deposited (t_2). (c) After NW trapping and formation of cross-linked APTES mask alignment marks, the flow set-up is dismounted for further NW contacting *via* UVL. (d) Representative SEM image of contacted SiNWs.

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PDMS[36] to seal the structure. Additionally, we do not plug the tubing into the PDMS stamp containing the microchannels, as this would strain the material. Instead, we first attach tubing to extra PDMS pieces, which are then bound to the main PDMS replica of the microchannels *via* self-adhesion.[36]

For depositing the UVL mask alignment marks, we use 3-aminopropyltriethoxysilane (APTES), which we bring into the channels for alignment mark deposition *via* capillary forces.[37] In a condensation reaction, the silane molecules bind covalently to the oxide surface of the silicon wafer substrate and cross-link among each other.[38] Consequently, solvent-resistant mask alignment marks remain on the substrate surface after dismounting the PDMS flow chamber (see Fig. 1c). The resistance of the alignment marks against organic solvents is important to prevent their dissolution during photoresist spin coating for subsequent UVL.

Using the APTES-based alignment marks, we deposit one pair of Ni contacts (source and drain) for each designated trapping site *via* UVL. A representative scanning electron microscopy (SEM) image of the contacted SiNWs is shown in Fig. 1d. All depicted devices are single-NW FETs. Up to 13 out of 32 designated trapping sites are occupied with single-SiNW FETs.

As determined in preliminary experiments, the deposited SiNWs are tilted by 21° ± 5° on average with respect to the wall of the inflow channel (see also Fig. S1e†). In the electrode design we take this tilt into account, as shown in Fig. 1d.

Fig. 2 summarizes the electronic properties of our SiNW FETs. In Fig. 2b the representative I_{SD}–V_{SD} characteristic of the highlighted single-SiNW FET (see Fig. 2a), with back gate architecture and 200 nm thick thermal SiO_2 as gate dielectric, is plotted. The characteristics show a p-type behavior of the devices, as expected for our p-doped SiNWs. However, average ON-currents of approximately 0.25 nA per single-SiNW FET are relatively low compared to other SiNW devices in literature,[7] which can be explained by two effects. First, the thick gate oxide and back gate geometry lead to a low gate coupling. Second, the commercial SiNWs utilized here are not passivated and thus charge trapping within the native oxide shell occurs, which effectively screens the gate efficiency (see Fig. S2†). For the future, we envision to apply our assembly method for the integration of NWs that are readily passivated, *e.g.* with thermal SiO_2 and high-*k* dielectrics, and that possess surrounding gate electrodes to overcome these issues.

However, there are also trapping sites where no SiNW or more than one SiNW is contacted. The averaged drain-currents of three different kinds of devices (0, 1 or 2 SiNWs per FET) are compared in Fig. 2c. As expected, the graph shows that output current scales with the number of SiNWs per FET.

Rarely, more than two SiNWs per trapping site are deposited, even if optical microscopy observations during the flow experiments indicate the trapping of an increased amount of SiNWs. We found that a large amount of trapped SiNWs is lifted off the receiver substrates upon dismounting the PDMS flow chamber (see Fig. S3†). We assume that mainly SiNWs having contact to the receiver substrate over their entire length stay on the surface. SiNWs having only partly or no contact to the substrate – *e.g.* due to lying on top of other SiNWs – are removed with the PDMS stamp due to adhesion forces.[36]

25–40% of our FET devices do not contain any SiNWs, 35–40% contain one SiNW, 15–25% contain two SiNWs, and below 10% contain more than two SiNWs. These yields are comparable to earlier works in this field, such as electric field-based NW alignment.[4,39] More recent electric field-based approaches[27] and EBL-supported deposition and contacting techniques[26] achieve significantly higher yields of single-NW devices. However, our approach unites simplicity, cost-efficiency and versatility.

To prove the versatility of our method we prepare a NW suspension from copper(II) oxide NWs (CuO NWs), grown as

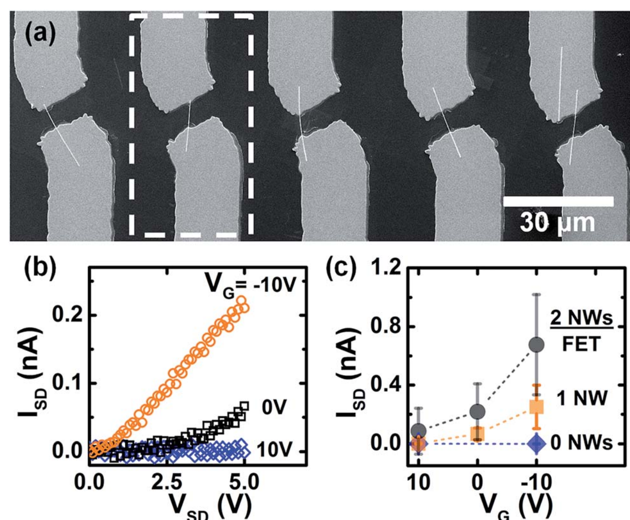

Fig. 2 (a) SEM image of five neighboring back gated single-SiNW FETs. (b) Representative single-SiNW FET I_{SD}–V_{SD} output curves recorded with the device highlighted in (a) at different gate voltages: orange circles, black squares, blue diamonds correspond to $V_G = -10$ V, 0 V, 10 V respectively. (c) Comparison of averaged drain currents in FET devices with different numbers of SiNWs at $V_{SD} = 5$ V: black circles, orange squares and blue diamonds correspond to 0, 1 and 2 SiNWs per FET, respectively.

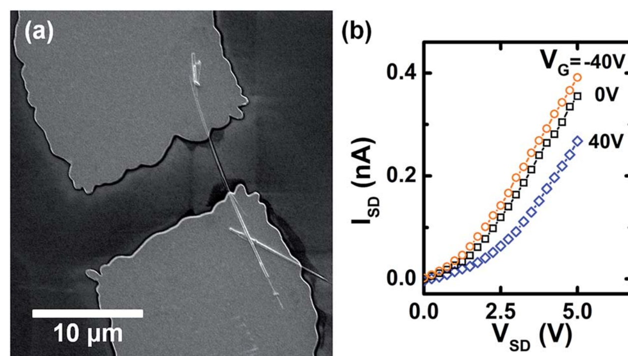

Fig. 3 (a) SEM image of a back gated single CuO NW FET fabricated with our approach. (b) I_{SD}–V_{SD} characteristics of the device shown in (a) at different gate voltages: orange circles, black squares, blue diamonds correspond to $V_G = -40$ V, 0 V, 40 V respectively.

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described elsewhere.[40] Fig. 3a shows a representative image of a CuO NW trapped and contacted with our approach. The plot in Fig. 3b demonstrates the p-type behavior of the CuO NW FET. The ON-current of 0.39 nA is in good agreement with the characteristics of other CuO NW devices in literature.[41]

Compared to the SiNWs, less single-NW FETs per chip are obtained when using the CuO NWs. We attribute this to the polydispersity of the CuO NWs in our suspension as well as to the fact that a large proportion of the CuO NWs is significantly shorter than the 20 μm-long SiNWs (see also Fig. S4†).

The results show that a monodisperse NW solution more likely yields single-NW devices. We assume, that NW concentration in suspension, the flow velocity at the trapping sites as well as the channel width and height at the trapping sites are also important parameters that will influence the yield of single-NW devices. In case of the trapping site geometry, reducing the channel height will guide the NWs closer to the receiver substrate surface on the bottom of the channel. This way they are more likely to assemble on the receiver substrate surface over their entire length, reducing the probability of receiving devices with no attached NWs. However, the probability of receiving devices with more than one NW is increased. Reducing the channel width again will decrease the amount of trapping sites where two or more neighboring NWs are deposited. However, reducing the channel dimensions (width and height, respectively) will make the system prone to clogging. This highlights that there is a delicate interplay of channel width and height towards the effective deposition of single-NW devices.

In conclusion, we have developed an approach based on continuous-flow microfluidics for the alignment, trapping and deposition of single NWs at designated positions, without limitations regarding NW materials. The option to use standard UVL for contacting the NWs renders the process cost-efficient and attractive for large scale applications. The fact that microfluidic channels with hundreds and thousands of trapping sites have been built for single-particle[29] and single-cell studies,[30] respectively, illustrates the upscaling opportunities of our method. Particularly in the field of chemo- and biosensing, the multiplexed detection of large amounts of analytes, as for example in DNA microarrays,[42] can be enormously enhanced with large-scale arrays of highly sensitive single-NW devices. Generally, as the positioning of 1D nanostructures can be fully controlled, our approach represents a simple, yet precise and versatile tool for integrating 1D "bottom-up" building blocks with their unique properties into "top-down" technology.

Abbreviations

1D	One-dimensional
APTES	3-Aminopropyltriethoxysilane
CuO NW	Copper(II) oxide nanowire
EBL	Electron-beam lithography
FET	Field effect transistor
NW	Nanowire
PDMS	Polydimethylsiloxane
SEM	Scanning electron microscopy
SiNW	Silicon nanowire
UVL	UV-lithography

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