Printable Parallel Arrays of Si Nanowire Schottky-Barrier-FETs with Tunable Polarity for Complementary Logic

Sebastian Pregl, André Heinzig, Larysa Baraban, Gianauronio Cuniberti Senior Member IEEE,
Thomas Mikolajick Senior Member IEEE and Walter M. Weber

Abstract — In this work we present a novel technology of printable bottom-up grown Si nanowire parallel arrays for low dissipation power electronics. Parallel aligned layers of monocrystalline Si nanowires can be deposited on arbitrary substrates over large areas by the printing process. The presented transistors consist of parallel arrays of longitudinal NiSi₂-Si-NiSi₂ nanowire heterostructures which naturally show ambipolar transistor behavior when a single gate is employed. By a double gate architecture, a reconfigurable transistor component is created, for which unipolar p- or n-type characteristics can be obtained depending on the polarity of the second gate. Transfer and output characteristics of these transistors on a Si/SiO₂ substrate with back gate, top gate and reconfigurable double gate architecture are presented here in detail. Very high on/off-current ratios of over 10⁸ are achieved with very low off-currents. Due to the high number of nanowires incorporated into individual parallel arrays, output currents of 0.5 mA and a high yield of functional transistors of close to 100% at nanowire coated areas are demonstrated.

Index Terms — silicon nanowire, reconfigurable transistor, parallel arrays, ambipolar, unipolar, intrinsic, undoped

I. INTRODUCTION

FUTURE market trends for next-generation consumer products demand lightweight, portable, low-cost and flexible electronics. A prerequisite for power saving electronics is the employment of a complementary transistor architecture which was introduced in 1963 and was ever since used to significantly reduce static power consumption in CPUs [1]. Circuits are built-up of pairs of networks of p-type and n-type (complementary) transistors connected in series. Either one of the transistors in the pair is in the off-state in the static case. Therefore, considerable power is only drawn during switching between on- and off-state, in contrast to pure PMOS or NMOS logic, which permanently consume electric power in the on-state. Such complementary logic circuits on flexible polymer substrates have been demonstrated with organic thin film transistors (OTFT) which are comprised of two different molecular building blocks for p- and n-type transistors [2, 3]. A low charge carrier mobility, low fabrication yield, increasing costs and substantial thermal long-term instabilities are major drawbacks of OTFT technology though [4]. Today, Si based electronics prevail the market of logic circuits, especially because of the low defect density of the interface of Si to its natural oxide SiO₂ serving as gate dielectric [5]. Charge carrier mobilities and reliability are much higher for Si based transistors than for OTFTs [6, 7]. Complementary polarities are commonly achieved by doping engineering for Si based technology. However, the high process temperatures needed for dopant activation and SiO₂ formation as well as technological difficulties to deposit monocrystalline Si on foreign substrates has limited the use of Si as semiconducting material for the application on thin film substrates.

Here we propose a technology, which is potentially able to integrate monocrystalline Si based complementary transistors on flexible substrates without the use of doping. By a printing process, bottom-up grown intrinsic Si nanowires are transferred from a Si growth substrate to arbitrary host substrates as a layer of parallel aligned nanowires [8]. Normal to the nanowire orientation, the electrodes are patterned and contact a large amount of nanowires in parallel increasing current output. This strategy works with a statistical distribution and density of nanowires and as such the device yield is high and exhibits a comparatively low device to device variance. In addition, there is no need of accurate positioning control as for individual bottom-up nanowires [9, 10]. We have demonstrated the printing capability and FET implementation on flexible polymer substrates for sensor applications [11]. Power saving logic circuits or driving stages for flexible displays are potential applications too. By using NiSi₂ metallic intruded contacts, undoped Si nanowire transistors exhibit ambipolar transfer characteristics, reflected in the capability to conduct n- and p-type charge carriers equally. Since this leads to an inability to turn off the devices, they are considered unsuitable for low dissipation power applications: off-currents and static power consumption are high. However, by a double gate architecture, ambipolar FETs can be reconfigured to unipolar FETs with high on/off-current ratio [12-19]. For these so called reconfigurable FETs...
(RFETs), the polarity can be switched from unipolar p-type or n-type depending on the voltage bias of the second gate, called program gate. The program gate selectively suppresses the injection of one type of charge carriers (e.g., holes), whereas the injection of the other charge carrier type (e.g., electrons) can be modulated via the second gate. On/off-current ratio and device performance can be increased significantly compared to ambipolar devices hereby. In previous publications we have demonstrated the world-wide first totally symmetric reconfigurable FET (RFET), which exhibits identical on-currents and subthreshold swing for p- and n-type polarity programs [19]. Hence, the two transistor components from conventional power saving CMOS technology can be mimicked by a single transistor building block. Circuit design is facilitated by only a single transistor type being required. A local dopant implantation and subsequent high temperature processes are not necessary since p- and n-type polarity can be adjusted electrostatically by the use of program gates. The highest temperature required is the silicidation anneal which can principally be kept as low as 280°C. Therefore, fabrication can be principally performed on polymer substrates with moderate glass transition temperature [11].

In section II, the ambipolar transfer characteristics of back gate and top gate devices are characterized individually for different gate lengths. The scaling properties of the most important DC transistor metrics are shown here. This knowledge is important to circuits with printed nanowires on host substrates. Section III presents the output characteristics and typical shortcomings of a low on/off-current ratio of ambipolar devices. In section IV we present the double gate reconfigurable transistor (RFET) with polarity control for which the two gates are realized by the back gate and top gate here.

II. BACK AND TOP GATE PERFORMANCE

In this section, transfer characteristics (I_{ds}, V_g) of the ambipolar devices with single back or top gate will be presented and discussed. The observed differences are explained on basis of the impaired electrostatic gate coupling of back gate devices with thick back gate oxide. Both transistor types are built of Si nanowires aligned in parallel bridging the source and drain (S/D) interdigitate contact leads (Figs. 1a,b). Lateral segments of the nanowires are silicided with Ni adjacent to the leads forming metallic NiSi2- Si - metallic NiSi2 heterostructures (Fig. 1b) as described in Section VI. Abrupt Schottky junctions are formed at the NiSi2 - Si nanowire interface. The back gate stack is realized by a degenerately p-doped Si / 400 nm SiO2 dielectric. For top gate devices, an Al2O3/Ni stack (20 nm/25 nm) is deposited on top of the back gate devices. Devices with a variation in inter electrode (IE) spacing of 4-16 µm are characterized. With 1.5 µm long NiSi2 segments from each electrode, this corresponds to Si channel lengths L of 1-13 µm.

Fig. 1d,e depict the schematic cross section of back gate and top gate devices together with the (I_{ds}, V_g) transfer characteristics with a typical ambipolar behavior. For the top gate device, the electric potential Φ_{ds} inside the Si nanowire conduction channel is both affected by the top and back gate voltages. A direct comparison between top and back gated devices reveals the following disparities:

1) Larger gate voltage values are needed for back gate devices to switch from the off- to the on-state, reflected in a larger subthreshold swing. This arises from a lower gate coupling due to the thick dielectric and planar gate geometry of back gate devices, compared to the thin Al2O3 high-k dielectric of top gate devices.

2) Back gate transfer characteristics are shifted to high positive gate voltages, which results from a very positive flat-band voltage V_{FB}. We attribute this to electron trapping at the nanowire surface which is covered by adhered H2O molecules at ambient conditions. As will be discussed below, the lower oxide capacitance of back gate devices leads to a larger impact of trapped negative charge on V_{FB}.

3) Subthreshold swing and on/off-current ratio are degraded towards smaller IE spacings, which is a result of an increasing electrostatic shielding of gate fields by the source/drain electrodes. The shielding effect increases for larger gate oxide thickness.

Fig. 1. Back gate and top gate ambipolar NiSi2-Si-NiSi2 SB-FETs: SEM image of (a) interdigitated electrode (IE) structures with 26 inter electrodes contacting 500-1000 nanowires, (b) close up of parallel aligned nanowires between two inter electrodes, (c) transistor after top gate stack (Al2O3/Ni) deposition. (d) Schematic cross section of Si nanowire SB-FET with intruded NiSi2 contacts on Si/SiO2 back gate stack. (e) Back gate transfer characteristics showing a degradation of the slope and on/off-current ratio with decreasing IE spacing. Deposition of Al2O3 front dielectric did not change the observed trends. Inset shows schematic nanowire cross section with electric potential Φ_{ds} dominated by trapped charge and source/drain potential at the surface (red) and back gate potential V_{bg} at the bottom (green). (f) Schematic cross section of nanowire SB-FET after top gate stack deposition. (g) Top gate transfer characteristics show IE spacing independent slope and high on/off current ratio. Larger low frequency CV-hysteresis can be observed in the n-branch, indicating electron trapping.
In the following, these individual points will be discussed in detail.

A. Gate coupling:
The electric potential $\Phi_{bg}(x=L/2)$ in the middle of the Si channel is modulated by the voltage of back gate $V_{bg}$ and top gate $V_{tg}$ according to their gate coupling factors $a_i$ [20, 21]:

$$\Delta \Phi_{eh}(x = L/2) = \Delta V_{bg} a bg = \Delta V_{bg} \frac{C_{bg}}{C_{bg} + C_d}$$

(1)

for the pure back gate devices without top gate stack and

$$\Delta \Phi_{ch}(x = L/2) = \Delta V_{bg} \alpha bg + \Delta V_{tg} \alpha tg$$

(2)

$$= \Delta V_{bg} \frac{C_{bg}}{C_{bg} + C_{tg} + C_d} + \Delta V_{tg} \frac{C_{tg}}{C_{bg} + C_{tg} + C_d}$$

for devices with top gate processed additionally on the front side. Here, $C_{bg}$ and $C_{tg}$ are the back and top gate oxide capacitance respectively, $C_d$ denotes the depletion layer capacitance at the drain side (the source side is neglected for simplicity). A high gate oxide capacitance is required to enhance the coupling of the respective gate. For a large gate oxide thickness $t_{ox}$ and low dielectric constant, oxide capacitance and gate coupling are low and as a consequence the subthreshold swing is impaired (high value). Since the back gate dielectric is 400 nm SiO$_2$ and top gate is 20 nm Al$_2$O$_3$, it follows $C_{bg} \ll C_{tg}$ and $a_{bg} \ll a_{tg}$. Equation (2) also shows, that a low back gate capacitance (thick $t_{ox}$) yields in an enhancement of the top gate coupling $a_{tg}$ and an electrostatically decoupling of $\Phi_{ch}$ from the substrate bias ($V_{bg}$). For the top gate device, electrostatics are dominated by the omega shaped top gate thus. The back gate potential hardly affects the top gate transfer characteristics.

B. Flat-band voltage:
Built-in potentials are summarized in the flat-band voltage $V_{FB}$ which can be expressed as [22]:

$$V_{FB} = \Phi_S - \Phi_{Si} - \frac{Q_f}{C_g} \frac{Q_n}{C_g} - \frac{1}{C_g} \int_0^{t_{ox}} \rho_{ox}(z)dz$$

(3)

where $C_g$ and $t_{ox}$ is the gate oxide capacitance and thickness, $\rho_{ox}(z)$ the oxide trapped charge density at the vertical distance $z$ from the gate, $Q_f$ and $Q_n$ oxide fixed and interface trapped charge, $\Phi_S$ and $\Phi_{Si}$ are the work functions of gate and intrinsic Si channel. Assuming a work function of $\Phi_{Si} = 4.6 \text{ eV}$ for the intrinsic Si channel, the similar work function of degenerately (boron) doped Si back gate ($\Phi_g \approx 5.0 \text{ eV} - 5.2 \text{ eV}$) and Ni top gate ($\Phi_{Ni} \approx 5.05 \text{ eV} - 5.15 \text{ eV}$ [23]) lead to a contribution between $+0.3 \text{ V}$ and $+0.6 \text{ V}$ to $V_{FB}$ for back and for top gate devices respectively. The main difference in $V_{FB}$ is caused by a combination of oxide charge and different capacitance values of the back gate $C_{bg}$ and top gate $C_{tg}$, with $C_{bg} \ll C_{tg}$. The oxide charge observed here is mainly negative in sign, resulting from a predominant electron trapping [24]. In back-gate devices lacking of top gate electrodes electrons tunnel through the surrounding nanowire oxide and are trapped at the nanowire surface, where H$_2$O molecules are adsorbed [36]. Previous results on silicon nanowire FETs involving vacuum desorption of H$_2$O molecules and hydrophobic surface functionalization have demonstrated a strongly reduced electron trapping and negligible flat band shift [37]. Electron trapping is also reflected in a stronger IV-hysteresis for the n-branch vs. the p-branch (Fig. 1e). Negative trapped charge at the nanowire SiO$_2$ shell is strongly promoting a positive $V_{FB}$ for back gate devices with small $C_{bg}$ as can be seen from (3). Furthermore, for the thick $t_{ox}$ (400 nm) and oxide trapped charge in the comparatively thin SiO$_2$ shell (8 nm) the last term in (3) can be approximated by $-Q_{ox}/C_{bg}$ since $z \approx t_{ox}$. The physical meaning is that the entire counter charge to $Q_{ox}$ accumulates in the Si channel and not in the gate. This represents the maximum possible effect of oxide trapped charge $Q_{ox}$ on $V_{FB}$, comparably strong to the effect of interface trapped charge $Q_f$. Hereby it is assumed, that charge trapping only occurs within the oxide shell surrounding the nanowire, not in the back gate dielectric, since the direct tunneling distance is typically of a few nanometers.

C. Electrostatic shielding by source/drain electrodes:
Fig. 2a-e illustrate the trends in the subthreshold region for top and back gate devices with different physical oxide thickness $t_{ox}$ at constant drain-to-source voltage $V_{ds} = -0.5 \text{ V}$. Top gate devices are characterized by a high on/off-current ratio with
low minimum currents $I_{\text{min}}$ and show similar $V_d(I_{\text{min}})$ for all IE spacings at low $V_{ds}$. The reasons are the comparatively small effective oxide thickness and high $C_{ox}$ which results in an effective control of the channel potential throughout the whole nanowire cross section for all IE spacings. In contrast, back gate transfer characteristics (see also Fig. 1c) show a significant decrease of on/off-current ratio (Fig. 2d), increase of $I_{\text{min}}$ (Fig. 2e) and degradation of subthreshold swing (Fig. 2h,c) for decreasing IE spacing. Further, $V_d(I_{\text{min}})$, for which the minimum current appears, shifts to more positive values as IE spacings decrease (Fig. 2a). This indicates that the back gate fields can hardly modulate the current for small IE spacing devices. This is not caused by classical short channel effects, since channel lengths ($L=1-13 \, \mu\text{m}$) are much larger than the depletion layer width [25, 26]. Also metallic fully silicidized nanowires, which would result in currents of $400 \, \mu\text{A}$ independently of the gate bias, are not present in any device. Instead, the degradation of back gate device performance with decreasing IE spacing can be explained by the increasing capacitative impact of source/drain contacts on $\Phi_{dh}$. Due to the low $C_{bg}$, the back gate potential is shielded strongly as the channel length is decreased and the back gate effectiveness is lost gradually. In turn, oxide trapped charge in the nanowire SiO$_2$ shell and source/drain potential will dominate $\Phi_{dh}$. Especially in the upper surface part of the nanowire cross section, $\Phi_{eh}$ is electrostatically dominated by negative oxide trapped charge (Fig. 1e inset). This leads to accumulation of holes and increased p-conduction which can hardly be turned off by the back gate for small IE spacings. As a result, the subthreshold swing of the p-branch is severely impaired. For very positive back gate voltages, which can efficiently turn off p-conduction at the surface part at the source contact, n-conduction is already turned on at the drain contact, which causes the observed increase in minimum current $I_{\text{min}}$.

D. Performance enhancement by downsizing size:
From Fig. 2b,c,e an improvement of the swing and on/off-current ratio by scaling down $t_{ox}$ is clearly visible. For the 20 nm Al$_2$O$_3$ dielectric, the actual values are independent from the IE spacing which shows a negligible influence of the source/drain contacts for the investigated channel lengths. However, the subthreshold swing of 200 mV/dec for the p-branch and 450 mV/dec for the n-branch are still not ideal, which is related to the relatively thick Al$_2$O$_3$ dielectric and the tunneling transport through the Schottky-barriers [27, 28]. On-currents are defined here as maximum currents achieved during $V_d$-sweeps and are depicted for top gate devices in Fig. 2f together with the peak transconductance values $g_{mn}$ in Fig. 2g. A non-linear increase of on-currents for shorter IE spacings is observed. The shorter source/drain separation for small IE spacings results in a reduced resistance of Si conduction channel, but also in higher electric fields at the Schottky- junctions [9, 29]. The electric field enhancement causes a reduction of the tunnel barrier width and thus an increase of the tunneling probability in the on-state [30]. The lower on-currents and larger swing for the n-branch are a result from the larger Schottky-barrier height for electrons $\Phi_{bn} = 0.66\, \text{eV}$ than for holes $\Phi_{bh} \approx 0.46\, \text{eV}$ and thus lower tunneling probability for electrons [31].

III. AMBIGIPOLAR DEVICE PERFORMANCE
In this section, the typical ambipolar operation of single gated Schottky nanowire FETs is demonstrated and explained for different biases. Although the high-off currents are impractical for classical circuit applications the basic operation mechanisms are important to elucidate the unipolar behavior in Section IV. Fig. 3a depicts the measured transfer characteristics of the ambipolar NiSi$_2$-Si-NiSi$_2$ SB-FETs operated by the top gate for various $V_{ds}$. Minimum currents $I_{\text{min}}$ achieved are strongly dependent on $V_{ds}$ and the current level in the off-state ($V_g=0\, \text{V}$) increases with $|V_{ds}|$. For ambipolar devices, the intersection point of n- and p-conduction branch determines the minimum current value $I_{\text{min}}$ and $V_{g}$-position $V_d(I_{\text{min}})$. To make this behavior plausible, Fig. 3d,e show TCAD simulated transfer characteristics for two different $V_{ds}$. The drain current contribution of holes and electrons is visualized separately to illustrate the curve shifts typical to Schottky barrier FETs as depicted in Fig. 2a.

![Fig. 3. $V_d$ dependence of minimum current $I_{\text{min}}$ for ambipolar SB-FETs, leading to on/off-current ratio degradation: (a) Transfer characteristics of top gate device (20 nm Al$_2$O$_3$/25 nm Ni) for various $V_{ds}$. A severe increase of $I_{\text{min}}$ and degradation of on/off-current ratio with increasing $|V_{ds}|$ is observed. $V_d(I_{\text{min}})$ depends on $V_{ds}$. (b) Output characteristics of top gate device. Majority carriers can switch between holes and electrons depending on $V_{ds}$. (c) Schematic band bending in dependence of nanowire conduction channel potential $\Phi_{dc} (\Phi_{dc} > V_d)$. (d,e) Simulated subthreshold characteristics for different values of $V_g$: Hole currents in red, p-branch and electron currents in blue. Dashed lines are thermionic emission only. Full lines are total current (thermionic and tunneling). Green lines show the total ambipolar current as a sum of the p- and n-currents. The intersection point of n- and p-branch determines the minimum current value $I_{\text{min}}$ and position $V_d(I_{\text{min}})$. For $\Phi_{dc} = V_g$ (knick in red curve) energy bands at the source/drain junctions are flat and hole tunneling is turned off. The details of the simulation have been described in [17].]
Electron (hole) conduction is steered by band bending at the drain (source) junction which depends on the difference $\Phi_{ds}$,$-V_d$ ($\Phi_{bg}$,$-V_d$) as illustrated by the schematic energy band diagrams in Fig. 3c. For $\Phi_{bg}(x=L/2)=V_d$, the bands at the drain junction are flat and electron tunneling is turned off. This point, indeed the whole n-branch, is shifted with the $V_d$ value (compare Fig. 3d,e). The p-branch is not affected since $V_i$ is constant. Hence, the intersection point of p- and n-branch is altered with $V_d$. For similar $\Phi_{bg}$ (0.46 eV) and $\Phi_{bn}$ (0.66 eV), minimum currents are expected for $V_{ds}$$<\Phi_{bg}$$<V_d$. In this case bands are bent downwards at drain and upwards at source which leads to tunneling of electrons from drain and holes from source into the channel simultaneously [32]. As an additional effect, larger absolute $V_d$ results in higher lateral electric fields across the Schottky- junction which reduces the tunneling barrier width. Thus, tunneling injection and $I_{min}$ are increasing further.

The measured output characteristics are plotted for this ambipolar transistor in Fig. 3b. The branches for p- and n- conduction cannot separately be displayed. Since overall current value and additionally $V_d$($I_{min}$) are altered with $V_{ds}$, the progression of the output curve is more complicated than for conventional unipolar devices. In the interval $0<V_{tg}<2$, the majority charge carrier can switch between holes and electrons by changing $V_{ds}$ (see also Fig. 3a).

IV. UNIPOLAR RFET DEVICE PERFORMANCE

Ambipolar transistors as shown in previous sections can be transformed into reconfigurable unipolar transistors (RFET) using a double gate architecture with program and control gate [12-19]. The RFET polarity can be switched from p- to n-type at runtime via the program gate which suppresses either hole or electron injection into the channel. Here, the role of the program gate is taken over by the back gate which controls the charge carrier injection directly at the Schottky-junctions. Current modulation is carried out by the control gate which is realized by a top gate here. The (meander shaped) top gate only covers the middle segment of the Si nanowire channel without overlapping the Schottky-junctions (Fig. 4a,b). An independent electrostatic control at Schottky-junctions and middle part of the Si conduction channel is thus enabled by $V_{bg}$ and $V_{tg}$. The local electric potential under the top gate at $x=L/2$ is governed by the omega shaped top gate since $\alpha_{bg}<\alpha_{tg}$, as can be seen from (2). At the Schottky-junctions ($x=L$, $x=0$), the back gate controls the nanowire channel potential due to the locally missing top gate. This effect was first reported for CNT transistors [16] and thereafter for top-down processed SOI nanowire transistors [14] with a similar gate geometry. At the location of the junctions it follows $\alpha_{bg}>>\alpha_{tg}$. A prerequisite is a large uncovered Si segment adjacent to the junction to avoid lateral electrostatic coupling from the top gate. Here, a device with channel length $L=13 \mu m$, $5 \mu m$ long uncovered Si segments and a mid-centered meander top gate of $2 \mu m$ width is used.

Fig. 4c depicts the unipolar p-type and n-type programs of the RFET together with the energy band profiles. The polarity is adjusted by the voltage $V_{bg}$ of the back gate (program gate). $V_{bg}$ steers energy band bending simultaneously at source ($x=0$) and drain ($x=L$) suppressing either hole or electron injection directly at the Schottky-junctions. By applying a positive $V_{bg}$ (here $+25 V$), energy bands at the source and drain junction are strongly bent downwards, decreasing the tunnel barrier width for electrons and suppressing p-conduction at the same time. In this case, the device is programmed as n-type FET (n-program). The n-current in this configuration is adjusted by the top gate voltage $V_{tg}$, which creates an additional energy barrier by local deformation of the electric potential in the channel middle. By varying this internal electric potential, n-conduction can be modulated by 8 orders of magnitude. The current modulation mechanism here is similar to a junctionless or accumulation-mode transistor: at positive $V_{tg}$, the whole Si channel is filled with electrons and can be depleted locally under the top gate for negative $V_{tg}$. The Schottky-junction
contributes independently of $V_{tg}$ with a constant (but $V_{bg}$ dependent) serial resistance. A p-type FET behavior (p-program) is obtained for negative back gate bias $V_{bg}$ (here -2V), when the energy bands at the source and drain junction are strongly bent upwards. The tunnel barrier width to and from the valence band is decreased giving a hole current and additionally n-conduction is efficiently suppressed. By the top gate, p-type current is modulated accordingly. High on/off-current ratios of $10^7$ are achieved.

Subthreshold swings of 175mV/dec for the p-branch and 135mV/dec for the n-branch are enhanced compared to ambipolar transistors shown in section II. The latter results from the different mechanisms of current quenching in the subthreshold regime. For ambipolar SB-FETs as in Figs.1,3 the shape of the Schottky barrier is modified by the gate potential. The differences are explained for n-type transport for simplicity. In the lower subthreshold region, where the conduction edge maximum in the channel is higher than the Schottky barrier height, the potential can be controlled linearly to $V_{cs}$, similar to the MOSFET thermionic shut-off mechanism. While the conduction band maximum beyond the flat band condition, the Schottky barrier exhibits a parabolic form with fixed height. Tunneling becomes dominant and the gate potential can only control the barrier thickness, therefore normally exhibiting a degradation of the subthreshold slope. [27]. In contrast, for the presented RFETs the shape of Schottky junctions are fixed by $V_{bg}$ and the charge carriers that already entered the channel are then filtered during shut-down by the movement of the top gate barrier as in a regular MOSFET. Hence, ideal swings of 60mV/dec can be theoretically achieved [13, 16]. Since un-doped Si is used and Schottky-barrier heights are comparable for n- and p-type charge carriers, the RFETs can be programmed almost symmetrically as p- or n-type FET. However, two different gate materials and oxide thicknesses are used here and locally different values of $V_{FB}$ at the Schottky-junctions (x = 0, x = L) and in the middle of the Si channel (x = L/2) are observed thus. At the Schottky-junction regions, the top gate is missing and oxide trapped charge strongly affects $V_{FB}$. Therefore, the flat-band voltage at the junctions $V_{FB}(x=0)$, $V_{FB}(x=L)$ shows a similar high positive value like for the presented back gate devices. The energy bands are initially bent upwards at the junctions (x = 0, x = L) for $V_{bg}=0V$, which results in a normally p-type transistor behavior. This explains the huge asymmetry in the required back gate voltage $V_{bg}$ to produce p-type (at $V_{bg}=-2V$) and n-type (at $V_{bg}=+25V$) polarity. In the channel middle, $V_{FB}(x=L/2)$ is expected to exhibit a value of close to 0V comparable to the presented single top gate devices. Therefore, conduction is normally turned-off for $V_{tg}=0V$ in both n- and p-type configuration. The device operates as accumulation mode transistor in both cases. For a fixed back gate voltage, the top gate n- and p-type transfer characteristics ($I_{ds}, V_{tg}$) exhibit very low hysteresis. The presented unipolar transistors are characterized by low off-currents and a high on/off-current ratio for all $V_{ds}$.

Output characteristics of the p-type and n-type programmed transistors demonstrate comparable characteristics to conventional accumulation-mode p-channel and n-channel MOSFETs (Fig. 4d,e). Pinch-off-like behavior and saturation region, analogue to conventional unipolar transistors, can be identified for both polarity programs. However, at low $|V_{ds}|$ below 1V, $I_{ds}$ increases non-linear with $V_{ds}$ especially for n-type polarity configuration. This is a typical effect observed for high and thick Schottky-barriers: since the majority of charge carriers are injected into the Si channel via tunneling, the Schottky-junctions represent a large serial resistance at low $|V_{ds}|$. For higher $|V_{ds}|$, the tunnel barrier width is reduced and the serial resistance, lumped here for both barriers into a to a single resistance $R_{SB}(V_{tg}, V_{ds})$, decreases. The overall resistance below saturation is composed of the channel resistance $R_{ch}(V_{tg})$ and $R_{SB}(V_{tg}, V_{ds})$:

$$R = R_{SB}(V_{tg}, V_{ds}) + R_{ch}(V_{tg})$$  (4)

For Ni$_2$Si-Si source and drain electrodes, the effect is stronger pronounced for n-type than for p-type polarity, since the Schottky-barrier height and thus the tunnel barrier thickness is larger for electrons than for holes. A linearization of the output conductance at low biases by proper scaling of the nanowire and oxide thicknesses and adjustment of the gate geometry has been discussed in [38].

V. SUMMARY AND OUTLOOK

SB-FETs consisting of bottom-up grown nanowires can be created with a high yield by assembly into parallel arrays. Thereby, the small current output of intrinsic Si based SB-FETs is enhanced significantly. A high yield of functional transistors of up to 100 % and output currents of 400 µA are achieved. NiSi$_2$-Si-NiSi$_2$ heterostructures, integrated with a single gate, show ambipolar behavior with low on/off-current ratio at high $V_{ds}$. By replacing the single top gate by a dual gate with separated control of the Schottky-junction region, the transistor polarity can be electrostatically adjusted. Unipolar and reconfigurable transistors (RFETs) with low off-current, high on/off-current ratio are obtained. On-currents can be enhanced significantly for future RFET parallel arrays via downscaling channel lengths and dielectric thickness as was shown here for single gate devices. Since both polarities can be achieved with an RFET, only a single transistor component type is needed to assemble complementary logic circuits. Although demonstrated with top gate and back gate here, RFETs can be realized with two individually addressable top gates [12, 17]. In this way, individual transistors can be addressed independently and reconfigurable complementary logic circuits can be produced. By the contact printing process, parallel arrays of bottom-up grown nanowires can be deposited on various substrates including polymer foils. Since high temperature processes can be performed before nanowire transfer, the fundament is laid down in this work to create RFET based low-operating power complementary logic on flexible substrates. This is expected to bring advantages also in terms of stable high temperature operation and stability to aggressive atmospheres, e.g. when integrated into chemo-sensors, as compared to conventional organic transistors.
In future, symmetry of n- and p-branch is pursued by strain engineering and using nanowires of smaller diameter [19]. However, the Schottky-barrier related serial resistance remains a drawback of the Si-based technology. By using an alternative intrinsic semiconductor like Ge with a low band gap, this serial resistance could be significantly reduced [17, 33]. Due to the separate control of p- and n-conduction, the RFET technology additionally promises high on/off-current ratio and low off-currents for Ge-based CMOS technology.

VI. FABRICATION

Bottom-up growth of nominally un-doped Si nanowires was performed with 20 nm Au seed particles and silane (SiH₄) as precursor in a CVD furnace as described elsewhere [9, 10]. Nanowires exhibit a diameter of 21 nm in average and are 40µm long. Growth direction was previously reported to be mainly <112> direction [34]. Contact printing is used to transfer nanowires from the growth substrate to a Si/SiO₂ substrate (degenerately p-doped/400 nm) which is the device chip substrate. During the printing transfer, nanowires are aligned in direction of printing, forming parallel aligned arrays [9, 10]. Areas of 2 cm² are covered by monolayers of directionally aligned nanowires with a high density. The AuSi eutectic tip of the nanowires is removed by selective etching in *agua regia* (HNO₃/HCl 1/3 v/v) for 4 hours. Nanowires are strongly attached to the substrate during the printing process and thus do not detach from the substrate during *agua regia* etching and cleaning processes. Etchant neutralization and cleaning is performed by rinsing with DI water, isopropanol and acetone. Subsequently, substrates are transferred to a rapid thermal processing (RTP) furnace for dry oxidation at 875°C for 6 min in O₂ atmosphere at a pressure of 1 bar. By this procedure, nanowires obtain a thermally grown SiO₂ shell with a thickness of approximately 8 nm [17, 19]. Inter digitated source and drain electrode patterns are fabricated on the nanowire layer covered areas by UV-lithographically using image reversal resist (AZ5214e) and lift-off technology. Before Ni deposition, the photoresist serves as an etch mask for removing the thermally grown oxide shell locally at the position of the electrodes. The etching is performed by immersion in 1% HF for 90 s. Sputter coating is employed to deposit 50 nm of Ni. Contacted to Ni electrodes after the lift-off, devices are annealed in a RTP furnace at 500°C in forming gas (H₂/N₂ 5/95 p/p) at a pressure of 1bar for 30 s. This procedure yields in a thermally driven silicidation of nanowires. Ni₅Si₃ segments are formed which expand in average 1.5 µm into the nanowire from each side of the electrodes. This shortens the Si channel segment length L of individual nanowires by 3µm, which corresponds to two times the average length of the intruded silicidized segments. The difference of IE spacing and channel length L can be seen from Fig. 1d, depicting schematically the cross section of the device. The interface of silicide and intrinsic Si channel was previously reported to be an abrupt and flat Ni₅Si₃-Si interface, avoiding local roughness induced electric field enhancement. As top gate dielectric, 20 nm Al₂O₃ is deposited on the entire chip surface by atomic layer deposition (ALD) with Tri Methyl Aluminium (TMA) as precursor using ozone for activation [35]. The process was performed in 150 cycles at 150°C with the following step parameters: introduction of TMA for 0.35 s, purging for 0.75 s, ozone (O₃) introduction and reaction for 15 s, purging for 10 s. Subsequently, UV-lithographical patterning is employed for local removal of Al₂O₃ by 1% HF etching over electrical contact pads and for deposition of the Ni (25nm) top gate electrodes. The top gate is produced in two variants: 1) a planar top gate, covering all transistor parts including nanowire, Schottky-junctions and source/drain electrodes and 2) a meander shaped gate of 2 µm width, covering only the middle part of the nanowire Si channel without overlap with the Schottky-junctions. For the second gate architecture, the Si/SiO₂ back gate stack is used to control electrostatics and electronic transport at the Schottky-junctions.

REFERENCES


