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Multiscale modeling of nanowire-based Schottky-barrier field-effect transistors for sensor applications

D Nozaki[1], J Kunstmann[1], F Zörgiebel[1], W M Weber[2], T Mikolajick[2] and G Cuniberti[1,3]

[1] Institute for Materials Science and Max Bergmann Center of Biomaterials, Dresden University of Technology, 01069 Dresden, Germany
[2] NaMLab gGmbH, Nöthnitzer Straße 64, 01187 Dresden, Germany
[3] Division of IT Convergence Engineering and National Center for Nanomaterials Technology, POSTECH, Pohang 790-784, Republic of Korea

E-mail: daijiro.nozaki@tu-dresden.de

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Abstract
We present a theoretical framework for the calculation of charge transport through nanowire-based Schottky-barrier field-effect transistors that is conceptually simple but still captures the relevant physical mechanisms of the transport process. Our approach combines two approaches on different length scales: (1) the finite element method is used to model realistic device geometries and to calculate the electrostatic potential across the Schottky barrier by solving the Poisson equation, and (2) the Landauer–Büttiker approach combined with the method of non-equilibrium Green's functions is employed to calculate the charge transport through the device. Our model correctly reproduces typical I–V characteristics of field-effect transistors, and the dependence of the saturated drain current on the gate field and the device geometry are in good agreement with experiments. Our approach is suitable for one-dimensional Schottky-barrier field-effect transistors of arbitrary device geometry and it is intended to be a simulation platform for the development of nanowire-based sensors.

S Online supplementary data available from stacks.iop.org/Nano/22/325703/mmedia

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Over the last few decades one-dimensional (1D) semiconducting silicon nanowires (SiNWs) have been widely studied as potential building blocks for future electronic devices due to their excellent electrical performance, small size, and controllable bottom-up fabrication [1–4]. Many types of SiNW devices such as ultrasensitive sensors [5, 6], photodetectors [7], and bipolar field-effect transistors (FETs) [8, 9] have been reported. The key issue for sensor applications is the downscaling of FETs to one-dimensional (1D) structures, such as nanowires. The attractive feature of nanowire-based FETs is that the binding of charged species can be directly monitored by the change in current through the nanowires because of their high surface-to-volume ratios and small cross-sectional conduction pathways.

Recently, Weber *et al* have reported dopant-free Schottky-barrier (SB) FETs consisting of intrinsic SiNWs working as a channel and $NiSi_2$ nanowires working as source and drain contacts with gate lengths down to sub-photolithographic values [10–13]. Their devices are based on single-crystalline SiNWs into which nickel atoms are diffusing from both ends of the wire, forming sharp interfaces between $NiSi_2$ 'leads' and a Si 'channel' in the center. The channel length depends on the annealing time. Measurements of their transport characteristics have shown the highest on-current and on-conductance values recorded to date for intrinsic SiNW-FETs. It is advantageous that the silicon channel is dopant free since the noise caused

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by structural impurities is greatly reduced compared to doped nanowires. This feature is beneficial for the production of reliable SiNW-based biosensors.

By modifying the surface of the SiNWs with DNA [14–16, 6, 17], enzymes [18] or other chemical compounds [5] many kinds of biosensors such as EnFETs (enzyme FETs), Immuno-FETs [19], and DNA-FETs have been demonstrated. Thus, SiNW-based SB-FETs are expected to provide a promising platform for biosensor applications.

For a better understanding of the basic charge transport characteristics through SiNW-based SB-FETs and the development of nanowire-based biosensors, it is essential to systematically reveal the factors controlling the charge transport through a pristine FET device.

Several approaches to describe the electronic transport through SB-FETs have been proposed. Matsuzaki *et al* developed a model to simulate charge transport through metal–oxide–semiconductor FETs (MOSFETs) with Schottky and Ohmic contacts using the Wentzel–Kramers–Brillouin (WKB) approximation and a triangular potential barrier [20]. Winstead *et al* made a model to analyze the I–V characteristics of MOSFETs using the Monte Carlo technique and an Airy function approach [21]. Knoch *et al* did quantum mechanical simulations of ultrashort channel n-MOSFETs on silicon on an insulator (SOI) [22] and of SB-FETs on SOI [23] using the real-space non-equilibrium Green's function formalism. Heinze *et al* introduced a method to calculate the transport through carbon nanotube (CNT)-SB-FETs using the Landauer formula and the WKB approximation [24]. This approach was expanded to coaxial gate CNT-SB-FETs by Guo *et al* [25, 26] and to cylindrical double-gate CNT-SB-FETs by Pourfath *et al* [27]. Appenzeller *et al* investigated the transport properties of a wide range of FETs such as CNT-FETs and SiNW-FETs in detail [28–30]. They used a modified 1D Poisson equation and the non-equilibrium Green's function technique to calculate the transmission function with the finite difference method in 1D. Jang *et al* simulated the I–V characteristics of SB-FETs using current continuity conditions [31]. Michetti *et al* expressed the conduction band by an analytical formula and calculated the transmission functions analytically [32]. Jimenéz *et al* expressed the conduction band profile with an analytical expression [33, 34] and calculated the transport properties of SB-FETs by using the WKB approximation, corrected with k-matching conditions for $MSi_2/Si(111)$ and $MSi_2/Si(100)$ (with M = Ni, Co, and Fe) interfaces [34].

The majority of these approaches were applied to highly symmetric devices such as cylindrical FETs or planar MOSFETs designed for integrated circuits. In these systems, the symmetry can reduce the computation time significantly. However, to simulate realistic devices for sensor applications with nanowires up to the μm scale, a computationally cheap model that is applicable to arbitrary device geometries is also desired. The multiscale model presented in this paper was developed for this purpose.

Our method combines two approaches on different length scales: (1) the finite element method (FEM) is used to calculate the three-dimensional (3D) electrostatic potential across the Schottky barrier by solving the Poisson equation for realistic device geometries. Then we extract the 1D potential profile along the axis of the nanowires and use (2) the Landauer–Büttiker approach combined with the method of non-equilibrium Green's functions [35–37] to calculate the charge transport through the device. To reduce the computational time, the transport calculation is divided into three processes: the tunneling through the Schottky barriers in the (1) left and (2) right interfaces and (3) the transport through the nanowire channel (see figure 2). Our model is conceptually simple, computationally inexpensive, uses only a few empirical parameters, and it is easily expandable. Since the method is non-atomistic the number of atoms in the system is irrelevant and therefore it is possible to simulate devices with dimensions ranging from a few nanometers up to some micrometers.

In this work we model pristine SB-FETs consisting of SiNWs and $NiSi_2$ NWs. We analyze the influence of the device geometries such as gate lengths, thickness of the insulators, and the gate voltages on the charge transport through the SB-FETs. Despite the simplicity of the model, the numerical calculations show I–V characteristics of typical conventional MOSFETs and the calculated saturation currents are in good agreement with the experimental results of Weber *et al* [10].

This paper is organized as follows. Section 2 presents the theoretical framework of our multiscale model and section 3 discusses the computational details and the parameter settings. In section 4 we study the dependence of the electrostatic potential on device geometries, investigate transmission profiles and I–V characteristics of test systems, and compare the numerical results with the reported experimental results. In order to show the general versatility of our method we also study a MOS-FET device and compare the results to the work of Knoch *et al* [23]. These results are provided as supplemental material (available at stacks.iop.org/Nano/22/325703/mmedia). Finally, we summarize this paper in section 5, emphasizing the simplicity and versatility of the multiscale modeling.

2. Theoretical framework

Figure 1 shows a schematic image of a SiNW-based SB-FET. The device consists of a SiNW working as a channel and $NiSi_2$ segments working as source and drain contacts. This nanowire is put on the gate contact covered with SiO_2. The source, drain, and gate voltages, V_S, V_D, and V_G, respectively, the nanowire diameter d_{NW}, as well as the length of the SiNW channel L_c, and the thickness of the oxide layer t_{ox} are all indicated in figure 1.

The band diagram of the electronic transport process through a SB-FET under an applied source–drain voltage with different gate voltages is shown in figure 2. The energy gap Φ_{SB} between the edges of the conduction band (CB) of the silicon channel and the Fermi energies of the $NiSi_2$ contacts is called the SB. The barrier thickness is reduced with increasing gate voltage, allowing the electron in the source to tunnel through the potential energy barriers [24, 38, 30]. Thus, the drain current at constant source–drain voltage is controlled by the gate voltage. The charge transport through the SB-FET can be divided into three stages (see figure 2): (1) electron

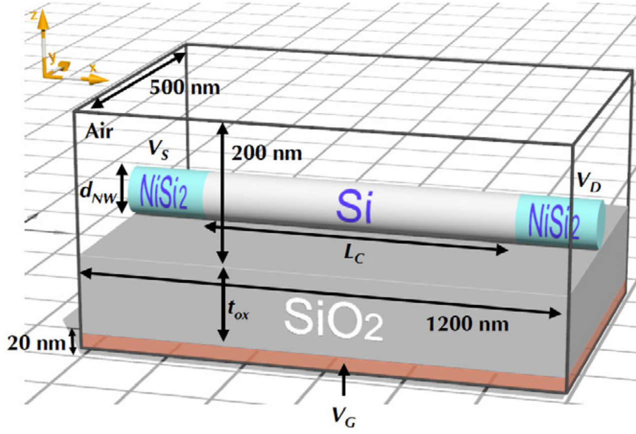

Figure 1. A model of a SiNW-based SB-FET with realistic dimensions, as considered in this work. V_S, V_D, V_G are source, drain, and gate voltages, respectively. L_c is the length of the SiNW channel, and t_{ox} is the thickness of the oxide layer. d_{NW} is the diameter of the SiNW.

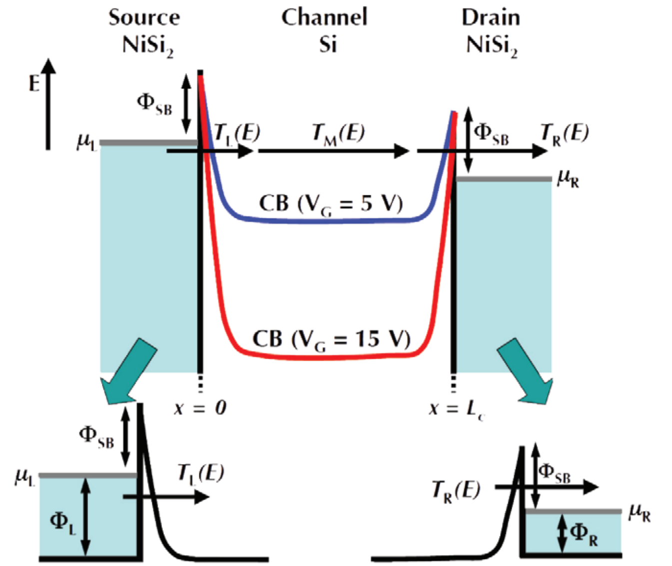

Figure 2. An energy diagram of a SiNW-based SB-FET under an applied source–drain voltage with different gate voltages V_G. The charge transport can be divided into three processes; coherent tunneling through the SB $T_{L/R}(E)$ at the left/right interfaces and ballistic transport $T_M(E)$ in the middle. Increasing the gate voltage leads to stronger bending of the conduction band (CB), which reduces the width of the SB. Φ_{SB} is the height of the SB. $\mu_{L/R}$ and $\Phi_{L/R}$ are the chemical potential and the ground potential for left/right contacts, respectively.

(hole) injection into the conduction band (valence band) by tunneling through the SB in the left interface; (2) ballistic or diffusive transport of charges through the SiNW; (3) tunneling of charges through the SB in the right interface.

According to figure 2 we define the 1D potential energy profile $U(x)$ along the axis of the $NiSi_2/Si/NiSi_2$ nanowire as

$$U(x) = \begin{cases} \mu_L - \Phi_L & \text{for } x < 0 \\ \mu_L + \Phi_{SB} + U_{ES} & \text{for } 0 \leqslant x \leqslant L_C \\ \mu_L - eV_{SD} - \Phi_R & \text{for } L_C < x \end{cases} \tag{1}$$

where the position $x = 0$ is set to be at the left $NiSi_2$ /Si interface, $\mu_{L/R}$ is the chemical potential of the left/right contact, Φ_{SB} is the SB energy, $\Phi_{L/R}$ is the ground potential for left/right contact, V_{SD} is the applied source–drain voltage, and $U_{ES}(x)$ is the 1D electrostatic potential along the axis of the SiNW obtained from FEM calculations (see below). For the SB energy Φ_{SB} we use experimental values from the literature (see below). The ground potential $\Phi_{L/R}$ is introduced in order to define the baseline for the transmission calculation at the two interfaces. The two ground potentials are chosen to span the bias window, i.e. $\Phi_L = eV_{SD}^{max}$, where V_{SD}^{max} is the maximum source–drain (bias) voltage that is used in a set of calculations, and $\Phi_R = 0$. In this way, the energy of the electrons in the source that are within the bias window is always higher than the ground potential. In order to calculate the charge transmission at the two interfaces (see bottom of figure 2) we use $U(x)$ in the interval $x = (-1.5 \text{ to } 21.5 \text{ nm})$ for the left and $x = (L_c - 21.5 \text{ nm}–L_c + 1.5 \text{ nm})$ for the right interface. In these two ranges the potential inside the SiNW ($0 \leqslant x \leqslant L_c$) is regularized by applying an energy cutoff U^{cut} such that $U(x) = U^{cut}$ for energies smaller than U^{cut}. At the left (L) and right (R) interfaces the cutoff energy is $U_{L/R}^{cut} = \mu_{L/R} - \Phi_{L/R}$, i.e. $U(x)$ is never smaller than the ground potential $\Phi_{L/R}$ (see also figure 5).

In this study, we employed the Landauer–Büttiker approach in real-space for the calculation of the electron transmission through the $NiSi_2$/Si interfaces [39–41, 30]. The Hamilton operator in 1D is given by

$$\hat{H} = -\frac{\hbar^2}{2m_{\text{eff}}} \frac{d^2}{dx^2} + U(x), \tag{2}$$

where m_{eff}, and $U(x)$ are the effective mass of electrons (or holes) and the potential energy profile along the axis of the nanowire, respectively. Using finite differences on an equally spaced grid, the Hamilton matrix is given by [40–42]

$$H_{n,m} = (U_n + 2t_0)\delta_{n,m} - t_0\delta_{n,m+1} - t_0\delta_{n,m-1}, \tag{3}$$

where $U_n = U(x_n)$ is the potential, $x_n = an$ is the position, a is the grid spacing, and $t_0 = \hbar^2/2m_{\text{eff}}a^2$.

The transmission functions at the left (L) and right (R) interfaces are obtained via the Landauer–Büttiker formalism using the Fisher–Lee relation:

$$T_{L/R}(E) = \text{Tr}[G^R \Gamma_{L/R} G^A \Gamma_M], \tag{4}$$

where Tr is the trace operation and Γ_α ($\alpha = $ L, R, M) are the broadening functions for the contacts, given by $\Gamma_\alpha(E) = \text{i}[\Sigma_\alpha(E) - \Sigma_\alpha^\dagger(E)]$. Γ_M is the auxiliary broadening function, which is required because the system is cut into two 1D tunneling problems. The self-energies are defined as $\Sigma_\alpha(E) = -t_0 \exp(\text{i}ka)$, where ka is obtained by inverting the band dispersion of the 1D wire (linear chain) $E(ka) = U_\alpha + 2t_0(1 - \cos(ka))$, and $U_\alpha = U(x_\alpha)$ ($\alpha = $ L, R, M) is the potential at the position of the left/right/auxiliary contacts [40–42]. Note that Σ_α is a diagonal matrix and its matrix elements are zero

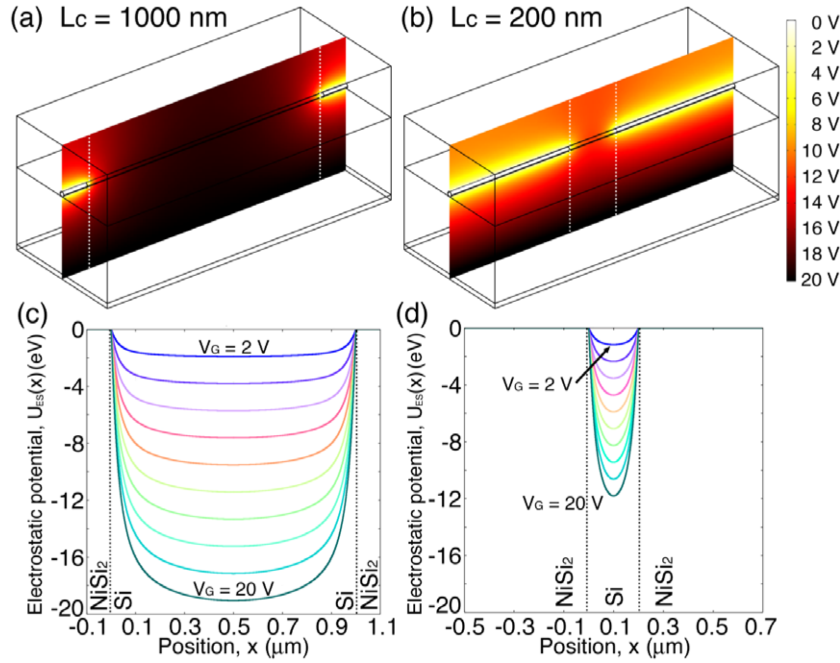

Figure 3. Electrostatic potential U_{ES} of the SiNW-based SB-FETs with different channel lengths being $L_c = 1000$ nm in (a) and (c) and $L_c = 200$ nm in (b) and (d). Top: $U_{\mathrm{ES}}(x, z)$ in the $y = 0$ plane; bottom: $U_{\mathrm{ES}}(x)$ along the axes of the corresponding wire. In these plots the metallic $NiSi_2$ nanowire is held at $U = 0$ V. The variation of the electrostatic potential is strongest close to the contacts.

except for the position where the left/right/auxiliary contact is attached.

The retarded/advanced Green's functions $G^{R/A}$ for the left (L) and right (R) interfaces are defined as

$$G^{\mathrm{R/A}}(E) = [(E \pm \mathrm{i}\eta)I - H - \Sigma_{\mathrm{L/R}} - \Sigma_{\mathrm{M}}]^{-1}, \quad (5)$$

where $\mathrm{i}\eta$ is an infinitesimal imaginary value, I is the identity matrix, $H = H_{n,m}$ is the Hamilton matrix, and Σ_α (α = L, R, M) are the self-energy matrices as defined above.

Assuming ballistic charge transport through the silicon channel, i.e. $T_{\mathrm{M}}(E) \simeq 1.0$, and ignoring the phase memory, the total transmission through the device is given by [40]

$$T(E) = T_{\mathrm{L}}T_{\mathrm{R}}/(T_{\mathrm{L}} + T_{\mathrm{R}} - T_{\mathrm{L}}T_{\mathrm{R}}). \quad (6)$$

The assumption of ballistic transport in the core channel region was validated experimentally for devices having channel lengths less than 1 μm [10]. In the presence of disorder or impurities the transmission through the channel will be reduced, i.e. $T_{\mathrm{M}}(E) < 1$. In this case $T_{\mathrm{M}}(E)$ can be calculated with classical or first principles methods and equation (6) has to be modified to include $T_{\mathrm{M}}(E)$.

Finally, the current through the SB-FET is calculated from

$$I_{\mathrm{SD}} = 2e/h \int_{-\infty}^{\infty} T(E)(F_{\mathrm{L}}(E) - F_{\mathrm{R}}(E))\,\mathrm{d}E. \quad (7)$$

The term $F_{\mathrm{L/R}}$ is the effective Fermi function k-summed over the transverse modes in the y–z plane, represented by

$$F_{\mathrm{L/R}}(E) = Sm_{\mathrm{eff}}k_{\mathrm{B}}T/\pi\hbar^2 \ln(1 + \exp((\mu_{\mathrm{L/R}} - E)/k_{\mathrm{B}}T)), \quad (8)$$

where S and $\mu_{\mathrm{L/R}}$ are the cross-sectional area of SiNWs and the chemical potential for left/right electrodes, respectively. Under an applied source–drain voltage V_{SD}, the chemical potential for the right electrode is given by $\mu_{\mathrm{R}} = \mu_{\mathrm{L}} - eV_{\mathrm{SD}}$.

Note that the same formalism works for hole currents by changing the band of interest from the conduction band (CB) to the valence band (VB), the Fermi function from $F_{\mathrm{L/R}}(E)$ to $1 - F_{\mathrm{L/R}}(E)$, the effective mass of an electron to the effective mass of a hole, and exchanging the sign of the gate voltages [33].

3. Computational details

In this work we assumed that the effective electron mass of the whole system for holes/electrons is equal to that of a free electron. For all calculations we use $\mu_{\mathrm{L}} = 0$ eV, $a = 1.0$ Å, $m_{\mathrm{eff}} = 1.0 \times m_{\mathrm{e}} = 9.109 \times 10^{-31}$ kg, and $T = 300$ K. For the discussion of electron transport and figures 3–6 we use $t_{\mathrm{ox}} = 300$ nm, $L_c = 1000$ nm, $d_{\mathrm{NW}} = 20$ nm, $\Phi_{\mathrm{SB}} = 0.50$ eV, and $V_{\mathrm{SD}}^{\max} = 0.5$ V, unless stated otherwise. For the discussion of hole transport and figures 7 and 8 we use $t_{\mathrm{ox}} = 300$ nm, $d_{\mathrm{NW}} = 21$ nm, $\Phi_{\mathrm{SB}} = 0.44$ eV, $V_{\mathrm{SD}}^{\max} = 2$ V. The 3D electrostatic potential $U_{\mathrm{ES}}(x, y, z)$ for each combination of V_{L}, V_{R}, and V_{G} is calculated by solving the Poisson equation with commercial FEM software (COMSOL Multiphysics [43]). The boundary potentials for the source, drain, and gate contacts are kept constant at V_{L}, V_{R}, and V_{G}, respectively. The finite element mesh for the modeled structures is automatically generated with controlled distribution and increased density in the regions close to the insulator and $NiSi_2$/Si interfaces. The 1D potential profile $U_{\mathrm{ES}}(x)$ in equation (1) along the axis of the nanowire is extracted from $U_{\mathrm{ES}}(x, y, z)$.

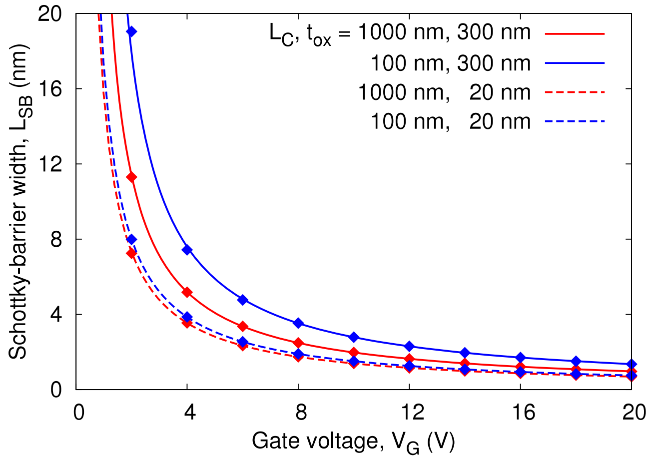

Figure 4. Dependence of SB width L_{SB} on the gate voltage V_{G}, the channel length L_{c}, and the thickness of the oxide layer t_{ox}. L_{SB} is defined in equation (9). The continuous lines are fits of the data points to $L_{\text{SB}} = cV_{\text{G}}^{-1}$, i.e., the SB width is inversely proportional to the gate voltage. The gate effect is most efficient for large channel lengths and thin oxide layers.

4. Result and discussion

4.1. Dependence of the electrostatic potential on device geometries

As a first examination of the relationship between the geometry of FET devices and the efficiency of the gate effect, we have calculated 3D electrostatic potentials of FET devices. Figures 3(a) and (b) depict the potential landscapes with a gate potential of $V_{\text{G}} = 20$ V and the absence of a source–drain voltage. Figures 3(c) and (d) show the same potential along the axes of the channels for long and short silicon channels, respectively. In figures 3(a) and (c), the potential along the silicon channel drops strongly due to the applied gate field, whereas the gate field does not penetrate efficiently in the shorter silicon channel in figures 3(b) and (d).

In addition we have analyzed the influence of the thickness of the insulating layer between the nanowire device and the gate on the SB width. The SB width L_{SB} of the left interface is defined by the position $x = L_{\text{SB}} > 0$ satisfying

$$U(L_{\text{SB}}) = \mu_{\text{L}}. \tag{9}$$

In figure 4, we show the SB width of the FET devices as a function of applied gate voltage with varying thickness of the gate insulators and the channel lengths. We can see that the gate field reduces the SB width for all devices. We find that the SB width is inversely proportional to the gate voltage. The reduction of the silicon channel length as well as an increase of the width of the oxide layer prevents the gate field from efficiently penetrating into the Schottky contact, leaving the width of the SB thicker than the device with a long channel or a thick oxide layer. Since the gate voltage narrows the SB the enhancement of the electron tunneling by the gate field is larger through SB-FET devices with longer silicon channels and thinner gate insulators [23, 25].

4.2. Transmission function and I–V characteristics

Figure 5 shows potential profiles $U(x)$ at the left interface for different gate voltages and the corresponding transmission functions $T_{\text{L}}(E)$ for electron transmissions through these SBs. The non-zero transmissions are due to the quantum tunneling effect. Since a positive gate voltage causes the SB to get thinner, the electron transmission increases with increasing gate voltage. For electrons with energies above the SB height Φ_{SB}, the electron transmission quickly approaches its maximum value of 1. Therefore our model takes into account both tunneling currents and thermo-activated currents (thermal emission) [20, 28, 31].

After calculating the transmission functions for both left and right interfaces, we have calculated the I–V characteristics of SB-FET devices by integrating over the total transmission function. Figure 6(a) shows the calculated drain current I_{SD} versus source–drain voltage V_{SD} for different gate voltages. The I–V curves show typical features of conventional FETs, i.e. a linear increase of current followed by current saturation for higher source–drain voltages. The saturation currents are strongly enhanced with increasing gate fields leading to a typical switching behavior with a high on/off-current ratio. We evaluated this behavior by calculating the drain current at a fixed source–drain voltage for several gate voltages.

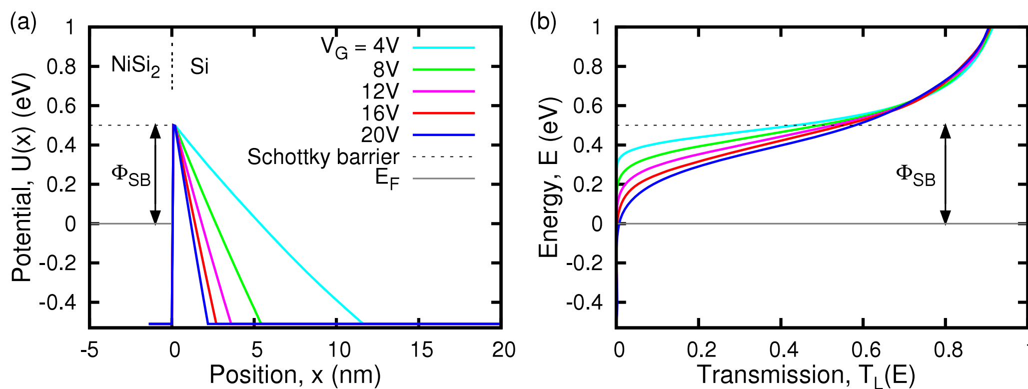

Figure 5. (a) The potential profile $U(x)$ across the central axis of the left $NiSi_2$/Si interface for different gate voltages V_{G}, and (b) the corresponding transmission functions $T_{\text{L}}(E)$. Here the SB height is $\Phi_{\text{SB}} = 0.50$ eV and the channel length is $L_{\text{c}} = 1000$ nm.

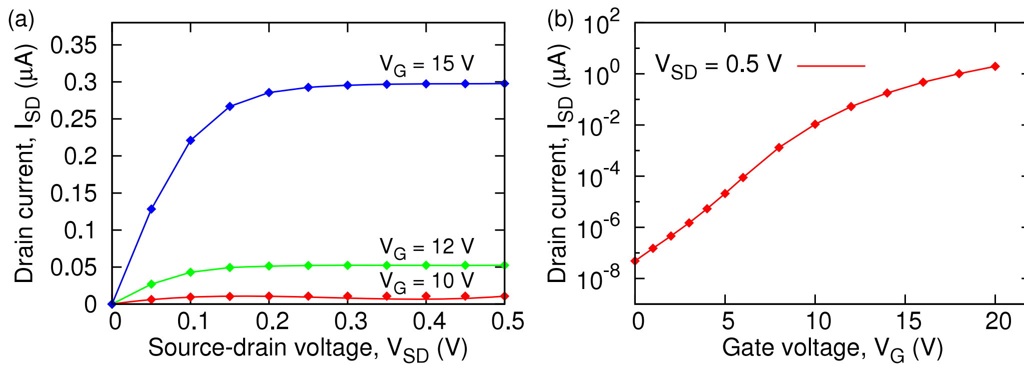

Figure 6. Electron transport characteristics of the SB-FET device with a channel length of $L_c = 1000$ nm and a SB height $\Phi_{SB} = 0.50$ eV. (a) Drain current I_{SD} versus source–drain voltage V_{SD} for different gate voltages V_G. The drain current saturates at higher bias voltages. The saturated current is significantly enhanced with higher gate voltages. (b) Drain current I_{SD} versus gate voltage V_G for a fixed source–drain voltage ($V_{SD} = 0.5$ V). We obtain the typical behavior of a conventional FET device.

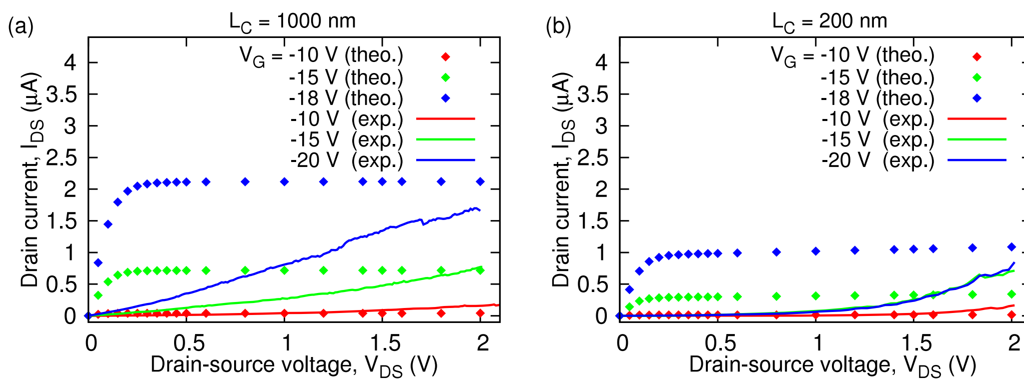

Figure 7. I–V characteristics of two FET devices for (a) a long and (b) a short channel length at different gate voltages. The calculated currents are shown with dots. The experimental results given by Weber *et al* [10] are shown as continuous lines for comparison. Although the theoretical currents reach their saturations at lower bias, the saturated currents show a good agreement with experiment. Note that $I_{DS} = -I_{SD}$ and $V_{DS} = -V_{SD}$.

Figure 6(b) presents the saturated drain current versus the gate voltage for a fixed source–drain voltage $V_{SD} = 0.5$ V. The drain current increases exponentially with the increase of the gate field in the lower gate voltages. This is due to the rapid reduction of the SB width with the increase of gate fields as shown in figure 4. The saturation of the drain current in higher gate fields can also be explained from figure 4 since the SB width does not decrease so much under higher gate fields. The huge on/off-current ratio implies that the device is promising for logic operations. The flatness of the current in the saturation region in figure 6(a) is also beneficial for the logic operation since the current remains constant with respect to fluctuation of the source–drain voltage.

4.3. Comparison with experiment

Many measurements of SB-FETs consisting of SiNWs have exhibited unipolar p-type transfer characteristics [10–13, 30], thus the current is transported by holes in these systems. As discussed previously, our model can also be applied to hole transport systems. In order to check the validity of the model, we have applied our model to SiNW-based SB-FETs and compared the I–V characteristics and on/off-current ratios with the experimental results measured by Weber *et al* [10].

The numerical parameters are set as follows. The SB height between Ni-silicide and bulk Si ranges from 0.35 to 0.47 eV for holes [44]. Thus, we set the SB height of the $NiSi_2$/Si interface for holes as $\Phi_{SB} = 0.44$ eV. The diameter of the SiNWs is set to $d_{NW} = 21$ nm, identical to the mean diameter of the literature [10]. The oxide thickness on the gate is set to $t_{ox} = 300$ nm.

Figure 7 presents the calculated drain currents I_{SD} versus source–drain voltage V_{SD} for (a) long ($L_c = 1000$ nm) and (b) short gate lengths ($L_c = 200$ nm) with experimental data provided by Weber *et al* [10]. The calculated I–V curves for both systems exhibit similar features to the experimental results, having both a linear increase and saturation at higher source–drain voltages. The drain current through the shorter channel is smaller than the one through the longer channel since the gate field does not optimally penetrate the $NiSi_2$/Si interfaces. Although the slopes of the calculated I–V curves for low source–drain voltages significantly exceed experimental ones, the value of the saturated drain current shows a good agreement with experiment except for the currents with high gate fields.

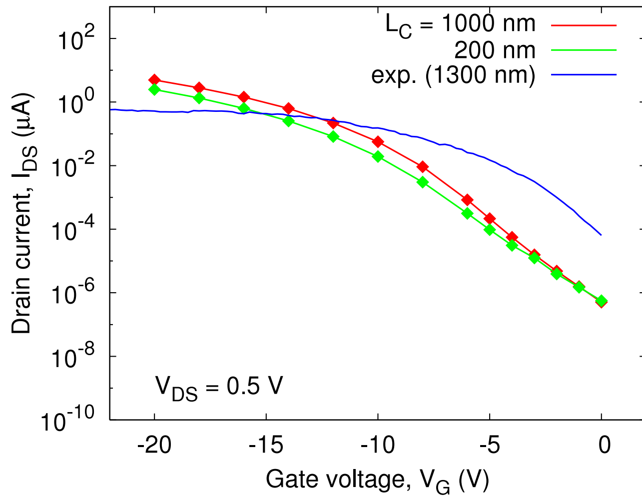

Figure 8. Drain current I_{DS} versus gate voltage V_G characteristics of SiNW-based SB-FET devices with long (in red) and short (in green) silicon channels. The source–drain voltage is fixed to be $V_{DS} = 0.5$ V. For comparison, the experimental results of Weber *et al* [10] for a long (1300 nm) SiNW are shown (in blue). The numerical results show a qualitative agreement with the experiment. In higher gate fields, the drain currents of the SB-FET with the long channel are higher than for the short channel because the gate effect is more efficient. In lower gate fields, the tunneling current is suppressed in both the long and the short channels, making thermal emission the dominating transport mechanism. Thus the drain currents through both long and short channels coincide.

Figure 8 presents the saturated drain current versus the gate voltage of SB-FET devices with long and short channels. The saturated drain currents increase significantly with the increase of the gate field since the gate field reduces the SB width as shown in figure 4. The on-currents in the short and long systems are of the same order of magnitude. Although the drain current in the lower gate field is underestimated, the numerical results show a qualitative agreement with experiment. Generally we observe that the drain currents of the SB-FET with the long channel are higher than for the short channel because the gate effect is more efficient (compare figures 3(c) and (d), 4, and 7(a) and (b)).

The discrepancies between our model and the experiment come from the simplicity of our model. First, we did not take into account the sub-bands [45, 34, 46] explicitly but merged them into a single band model. The inclusion of the sub-bands will lower the drain current for small source–drain voltages since the onset of current flow through the channel will be shifted to higher source–drain voltages due to the difference in energies between sub-bands. In addition, the reconstruction of the exact potential profile at the Schottky contact [47, 48] due to space–charge effects and the dependence of the potential on the lateral position in the wire are not considered in this study. Furthermore, the effect of capacitance at the left and right interfaces and at the gate contact are not included [49]. The addition of a native SiO_2 layer on the surface of the nanowire and the corresponding change of the electronic structures between the core and surface of the nanowire will also have an impact on the transport properties [50]. In principle, the influence of electron–electron or electron–phonon interactions on the charge transport can be studied by adding perturbative terms to equations (2) and (5) [26, 51]. In order to capture the underlying physics of SB-FET devices, an advanced model incorporating these effects will be needed. Further studies including these effects will give helpful information for the future development of nanowire-based FET devices.

5. Conclusion

In summary, nanowire-based FETs have been focusing attention as a promising platform for sensor applications due to their high sensitivity. In order to understand the origin of the physical behavior in nanowire-based FET devices, we have developed a multiscale model combining classical FEM and the Landauer–Büttiker approach. Our model is conceptually simple and computationally inexpensive, it uses only a few empirical parameters, and it is possible to simulate devices with dimensions ranging from a few nanometers up to some micrometers. We have applied this model to SB FETs consisting of SiNWs working as a channel and $NiSi_2$ NW working as source and drain contacts and to a MOSFET device, discussed in the supplemental material (available at stacks.iop.org/Nano/22/325703/mmedia). Our calculated I–V characteristics for the SiNWs showed behavior typical of conventional FET devices, having a linear increase of current followed by a saturation. The saturated drain currents increase with increasing gate field due to the reduction of the SB width. Despite the simplicity of the model, the calculations showed a good agreement with experiments and the model correctly reproduces the dependence of the saturated drain current on the gate field and the device geometry.

Our approach is suitable for one-dimensional SB field-effect transistors of arbitrary device geometry. The model can be improved by taking into account for example insulating layers surrounding the nanowires, the deformation of the electrostatic potential at the Schottky contacts, accurate electronic band dispersions, or non-ballistic transport through the Si channel. The results obtained from our model will serve as guidelines for the understanding of ongoing experimental work and will help in the design of device architectures for future applications.

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